Exhibit

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seeq

PRELIMINARY DATA SHEET

48F512
512K FLASH™ EEPROM

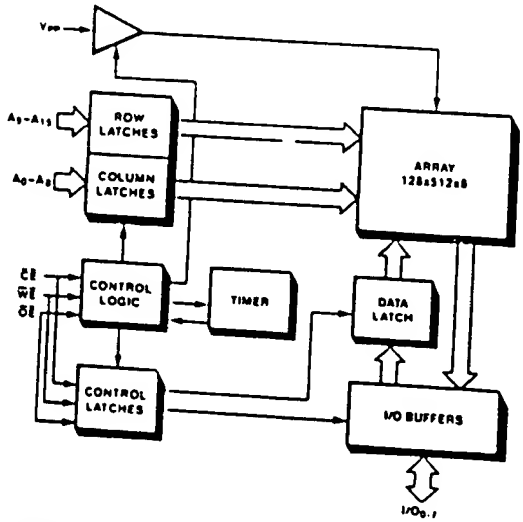
October 1988

FLASH

Features

- 64K Byte FLASH Erasable Non-Volatile Memory
- Low Power CMOS Process
- Electrical Byte Write and Chip/Sector Erase
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- FLASH EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
  - Minimum 100 Cycle Endurance
  - Optional 1000 Cycle Endurance Screening
  - Minimum 10 Year Data Retention
- 5V ± 10% V_{CC}, 0°C to +70°C Temperature Range
- Silicon Signature®
- JEDEC Standard Byte Wide Pinout
  - 32 Pin DIP
  - 32 Pin J-Bend Plastic Leaded Chip Carrier

Block Diagram



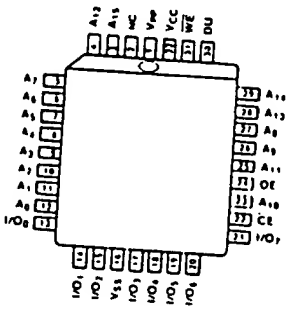
Pin Names

A_0-A_8	COLUMN ADDRESS INPUT
A_8-A_{15}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

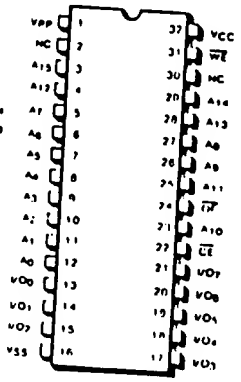
Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Pin Configurations

PLASTIC LEADED CHIP CARRIER TOP VIEW



DUAL-IN-LINE TOP VIEW



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Description

The 48F512 is a 512K bit CMOS FLASH EEPROM organized as 64K x 8 bits. SEEQ's 48F512 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each sector containing 512 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the 48F512 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_9 through A_{15}. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time t_{ABORT} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{ABORT} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the 48F512 in a group of bytes called a sector. The memory array is divided into 128 sectors of 512 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

Sectors are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. After 10 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm. the number of loops required. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

This device contains a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 48F512 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code 48F512	V_{IH}	1A

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{9-15}	A_{0-8}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:

Storage . . . . . −65°C to +125°C

Under bias . . . . . −10°C to +85°C

All inputs except V_{PP} and outputs with Respect to V_{SS} . . . +7 V to −0.5 V

V_{PP} pin with respect to V_{SS} . . . . 14 V

E.S.D. Characteristics[1]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested

FLASH

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Recommended Operating Conditions

	48F512
V_{CC} supply voltage	5V ± 10%
Temperature range	0°C to 70°C (ambient temp.)

Capacitance[2] (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN} = 0 V
C_{OUT}	Output capacitance	12 pf.	V_{OUT} = 0 V

Note 2: This parameter is only sampled and not 100% tested.

DC Operating Characteristics

Over the V_{CC} and temperature range

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{IH}	Input leakage high		1	µA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	µA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	µA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current				
	Standby mode		200	µA	$\overline{CE} = V_{IH}, V_{PP} = V_P$
	Read mode		200	µA	$\overline{CE} = V_{IL}, V_{PP} = V_P$
	Byte write		40	mA	$V_{PP} = V_P$
	Erase		80	mA	$V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current	CMOS	100	µA	$\overline{CE} = V_{CC} - 0.3$ v
I_{CC2}	Standby V_{CC} current	TTL	5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		60	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH1}	Output level (TTL)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output level (CMOS)	$V_{CC}-0.4$		V	$I_{OH} = -100\mu A$

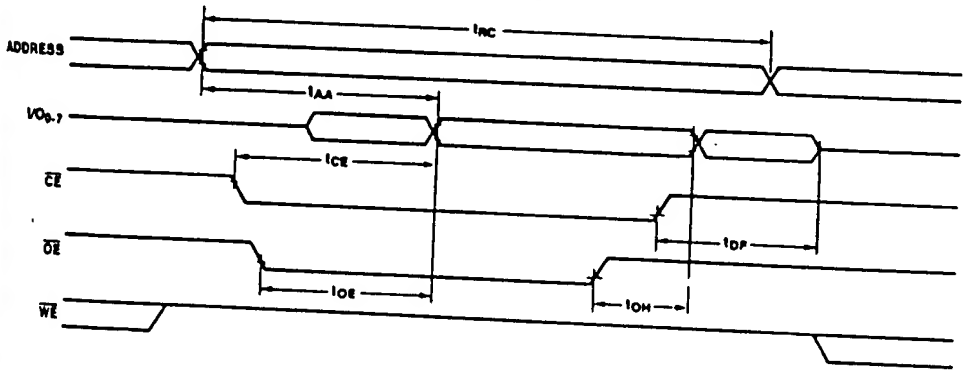
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	200		250		300		ns
t_{AA}	Address to data		200		250		300	ns
t_{CE}	$\overline{CE}$ to data		200		250		300	ns
t_{OE}	$\overline{OE}$ to data		75		100		150	ns
t_{DF}	$\overline{OE}$/$\overline{CE}$ to data float		50		60		100	ns
t_{OH}	Output hold time	0		0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics

(Over the V_{CC} and temperature range)

BYTE WRITE

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	250		250		250		µs
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	10		10		10		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{WC}	Write cycle time	100	150	100	150	100	150	µs
t_{WR}	Write recovery time		1.5		1.5		1.5	ms

Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g. access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Byte Write Timing

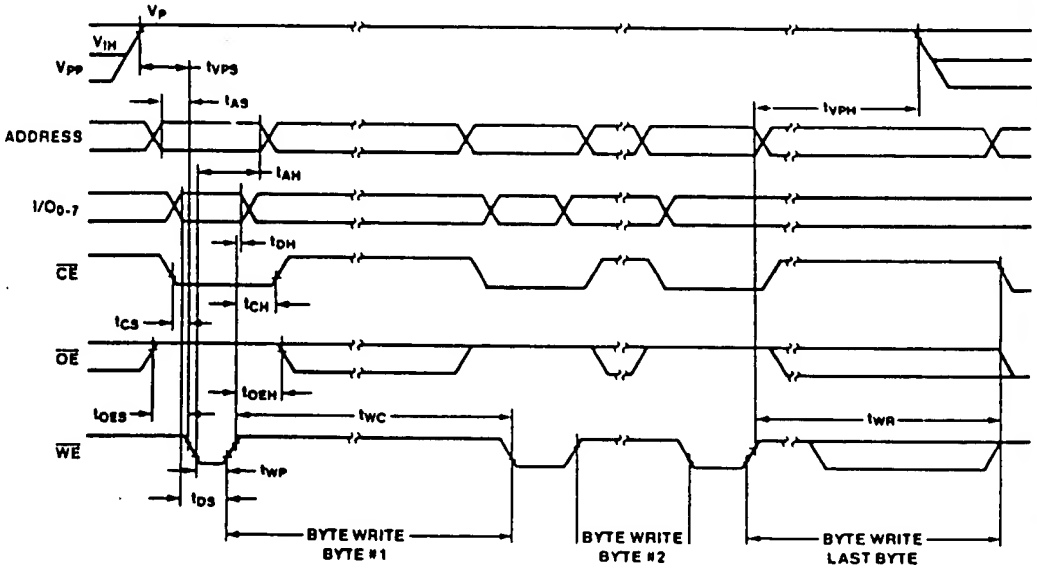
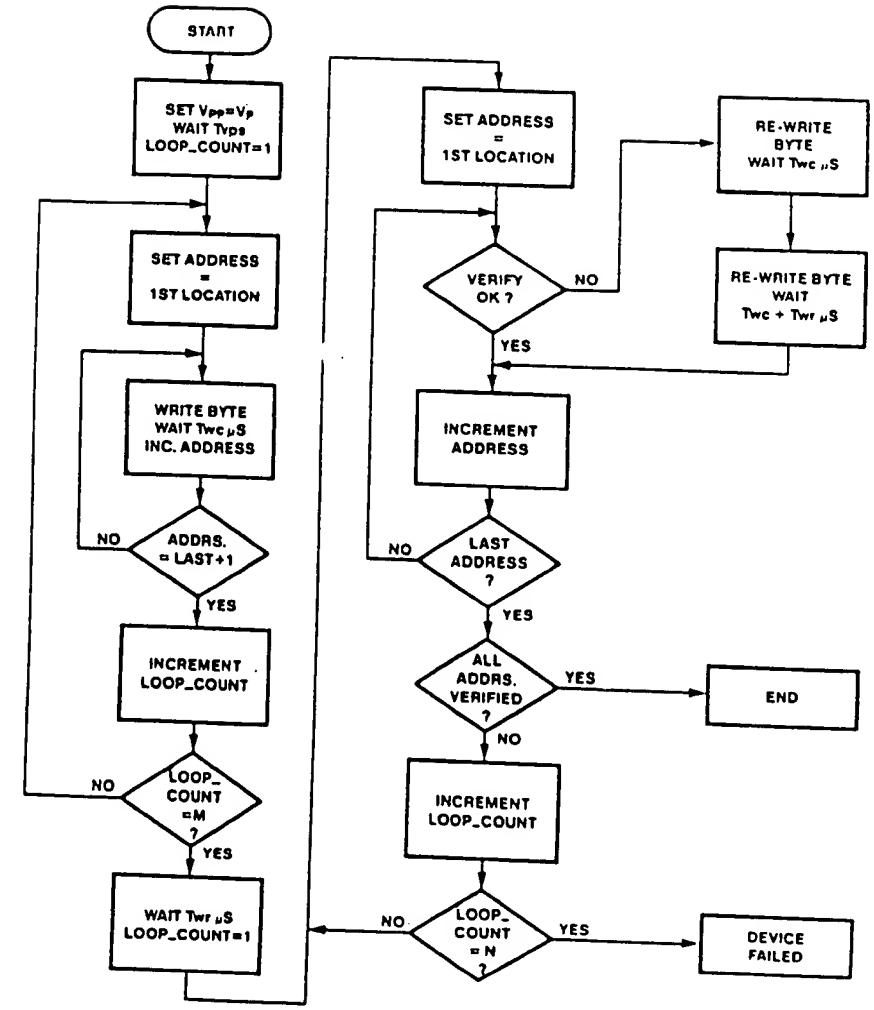


Figure 1
48F512 Write Algorithm



AC Characteristics

(Over the V_{CC} and temperature range)

SECTOR ERASE

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Sector erase time		500		500		500	ms
t_{ABORT}	Sector erase delay		250		250		250	µs
t_{ER}	Erase recovery time		250		250		250	ms

Sector Erase Timing

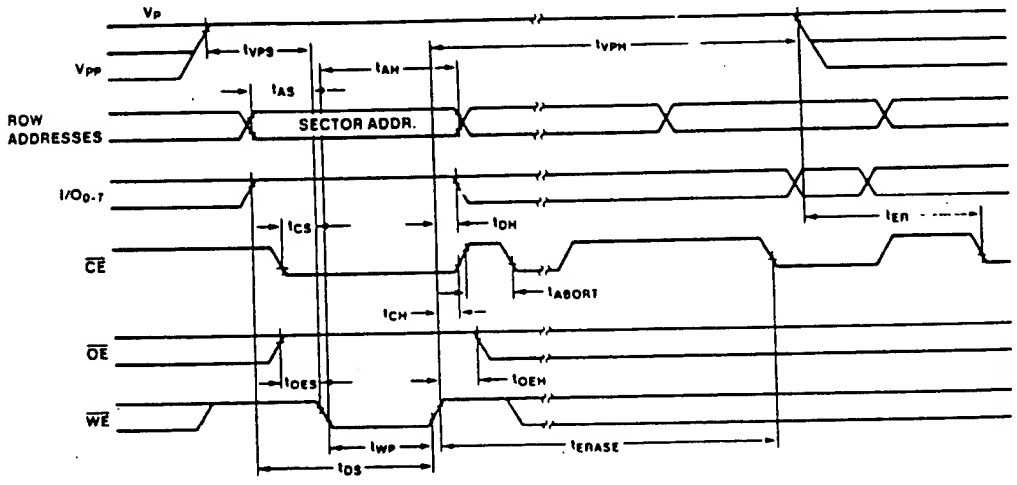
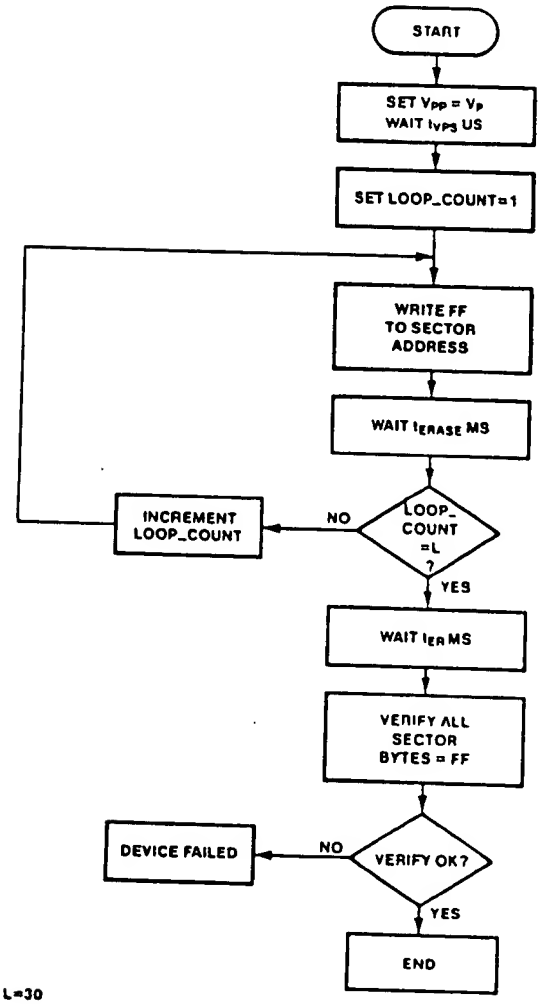


Figure 2
48F512 Sector Erase Algorithm



AC Characteristics

(Over the V_{CC} and temperature range)

CHIP ERASE

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Chip erase time		500		500		500	ms
t_{ER}	Erase recovery time		250		250		250	ms

Chip Erase Timing

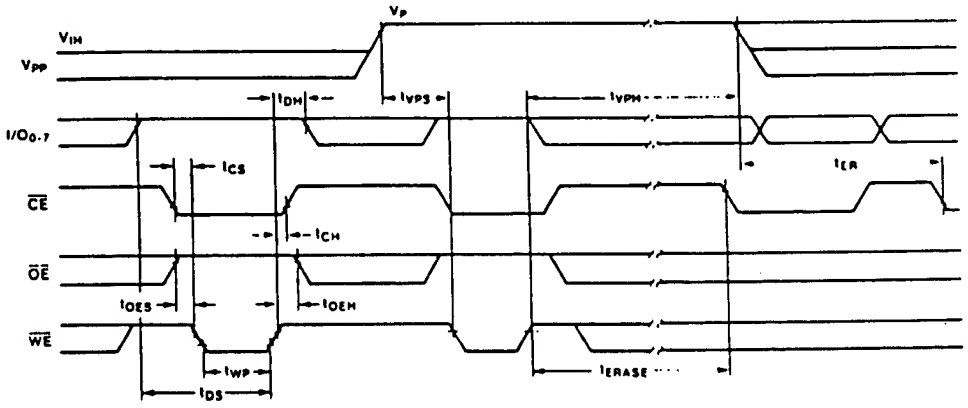
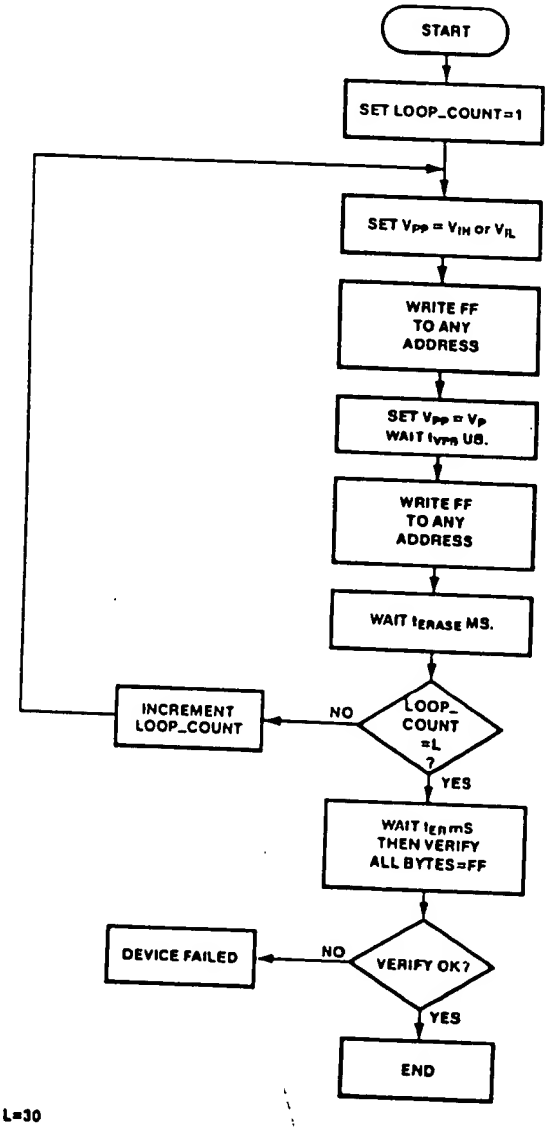


Figure 3
48F512 Chip Erase Algorithm



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